the Examiner contends that Lim teaches an integrated circuit comprising "a conductive layer (112) formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer (12) at a plurality of points spaced throughout the buried layer" (final Office Action; page 2, last paragraph). The Examiner further contends that it is inherent that the conductive layer disclosed in Lim reduces an effective lateral resistance of the isolation buried layer to thereby increase an electrical isolation between the first and second circuit sections (final Office Action; page 2, last paragraph to page 3, first paragraph). Applicant respectfully disagrees with these contentions.

Applicant submits that claim 1 of the present application requires that the conductive layer be coupled to the isolation buried layer "at a plurality of points spaced throughout the buried layer." The Lim reference fails to teach or suggest this limitation. Rather, with reference specifically to FIG. 2, Lim clearly discloses deep trenches (33 or 38) filed with P+ doped polysilicon material forming an isolation ring surrounding, and in electrical contact with, the periphery of a corresponding buried layer (12 or 13, respectively) (Lim; column 3, lines 62-64; column 4, lines 6-10). While Lim may disclose a silicide layer (112) "formed on the exposed portions of trench fill polysilicon 33 and 38" (Lim; column 8, lines 23-25), Lim fails to disclose that the buried layer is coupled to a conductive layer on the surface of the integrated circuit (IC) at a plurality of points. Furthermore, Lim clearly fails to teach or suggest that the conductive layer is coupled to the buried layer at multiple points spaced throughout the buried layer, as required by the claimed invention.

Even assuming, *arguendo*, that the silicide layer (112) disclosed in Lim can be analogized to a conductive layer on the surface of the IC, and assuming further that the buried layer (12) in Lim is coupled to the conductive layer via the polysilicon isolation ring (33), Applicant submits that the isolation ring taught by Lim is only in electrical contact with, at most, an edge of the buried layer, and not coupled to the buried layer at a plurality of points spaced throughout the buried layer. Thus, a lateral (i.e., sheet) resistance across the buried layer, e.g., between a center and an edge of the buried layer, in Lim is not significantly reduced. Moreover, the ring structure connected along the edge (i.e., periphery) of the buried layer disclosed in Lim cannot, by definition, be connected to the buried layer at a plurality of points spaced throughout the buried layer, as required by the claimed invention.

Applicant submits that an important aspect of the claimed invention is that, by connecting the isolation buried layer to the conductive layer at multiple points spaced throughout the isolation buried layer, the effective lateral resistance across the buried layer, between any two points in the buried layer, is substantially reduced. This objective cannot be accomplished if connection to the buried layer is made only at the edges, as in Lim. This is further explained in the present specification, where it states: "Preferably, the distance between any two plugs is close enough such that the isolation buried layer is sufficiently connected to the conductive layer, preferably in a substantially uniform manner" (specification; page 12, lines 20-22). By contrast, Lim discloses a localized isolation or shielding structure which employs a polysilicon ring around the periphery of a buried layer. The isolation ring surrounding the periphery of the buried layer, as taught by Lim, cannot reasonably be analogized to "a plurality of points spaced throughout the isolation buried layer," as set forth in claims 1 and 26 of the present invention. The isolation techniques of the claimed invention offer superior results not obtainable with the techniques disclosed in the prior art of record.

Furthermore, since Lim does not teach or suggest a buried layer that is coupled to a conductive layer on the surface of the IC at a plurality of points spaced throughout the buried layer, the effective lateral resistance (e.g., between the center and an edge) of the buried layer in Lim is substantially unchanged. Thus, the arrangement taught by Lim does not inherently reduce the effective lateral resistance of the buried layer, as the Examiner contends (final Office Action; page 2, last paragraph to page 3, first paragraph).

Inasmuch as Lim fails to teach or suggest at least a conductive layer formed on the surface of the IC that is "coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer," as required by claims 1 and 26, Applicant respectfully submits that claims 1 and 26 are patentable over the Lim reference. Accordingly, favorable reconsideration and allowance of claims 1 and 26 are respectfully solicited.

With regard to claims 2, 6-9 and 13-16, which depend from claim 1, and claims 27-29, which depend from claim 26, Applicant respectfully asserts that these claims are also patentable over the prior art by virtue of their dependency from their respective independent claims, which are believed to be patentable for at least the reasons set forth above. Moreover, one or more of these claims

define additional patentable subject matter in their own right. Accordingly, favorable reconsideration and allowance of these claims are respectfully requested.

Claims 3-5, 10-12, 17, 26-29, 30 and 31 stand rejected under §103(a) as being unpatentable over Lim. With regard to claim 3, for example, the Examiner acknowledges that "Lim et al. differ from the claimed invention by not showing the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net" (final Office Action; page 4, last paragraph). However, the Examiner contends that it would have been obvious to a person having skill in the art to form the conductive layer in the manner claimed "because it depends on the amount of noise that need [sic] to be reduced" (final Office Action; page 5, first paragraph). Applicant respectfully disagrees with this contention. In this regard, Applicant asserts that a motivation for using a conductive layer comprising a conductive net set forth in claim 3 is not to reduce the amount of noise, as the Examiner contends. Rather, the conductive net is used primarily to reduce a lateral resistance of the buried layer, which Lim fails to teach or suggest. Any noise reduction which may result from such arrangement is secondary.

Applicants assert that claim 26 was similarly rejected under §102(e) based on the Lim reference. Since the Examiner acknowledges that "Lim et al. do not teach a semiconductor device formed on a semiconductor wafer" (final Office Action; page 7, paragraph 4), the rejection of claim 26 under §102(e) is believed to be improper. However, since claim 26 is similar in scope to claim 1, Applicant asserts that claim 26 is believed to be patentable over Lim for at least the reasons set forth above, and therefore favorable reconsideration and allowance of claim 26 are respectfully requested.

With regard to claims 3-5, 10-12 and 17, which depend from claim 1, and claims 27-29, which depend from claim 26, Applicant submits that these claims are also patentable over the prior art by virtue of their dependency from their respective claims. Furthermore, one or more of these claims define patentable subject matter in their own right. For example, claim 3 further defines the conductive layer of the present invention as comprising "a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net." Applicant submits that Lim fails to teach or suggest at least this limitation, and that such required modification of Lim would not be obvious to one skilled in the art.

It is well established that a showing of a suggestion, teaching, or motivation to combine prior art references or to modify a prior art reference is an essential component of an obviousness holding, and that such suggestion or teaching must come from the prior art. *See, e.g., C.R. Bard, Inc. v. M3 Systems, Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998). The best defense against the improper use of a hindsight-based obviousness analysis is "rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). It is improper, in determining whether one of ordinary skill in the art would have been led to modify Lim in the manner suggested by the Examiner, "simply to [use] that which the inventor taught against its teacher." *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-313 (Fed. Cir. 1983). The obviousness rejection must be based on evidence of record, and the Examiner must also explain the reasoning by which the findings are deemed to support the Examiner's conclusions. *See, e.g., In re Sang-Su Lee*, 277 F.3d 1338, 1344 (Fed. Cir. 2002).

As previously noted, with regard to claim 3, the Examiner acknowledges that Lim fails to disclose that the conductive layer comprises a plurality of conductive traces interconnected with one another to form a net. However, the Examiner incorrectly contends that such arrangement would be obvious. Since Lim fails to teach or suggest any reason to reduce the lateral resistance of the buried layer, it would not be obvious to form a conductive layer on the surface of the IC in the manner claimed. In fact, forming a conductive net over the IC, as recited in claim 3 of the present invention, considerably reduces the circuit density of the IC. Therefore, absent a stated justification for doing so, which Lim clearly fails to provide, it would be undesirable to modify Lim so as to form a conductive layer on the surface of the IC comprising a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net, as required by the subject claim.

For at least the foregoing reasons, Applicant asserts that claims 3-5, 10-12, 17 and 27-29 are patentable over the prior art of record, not merely by virtue of their dependency from their respective claims, but also in their own right. Accordingly, favorable reconsideration and allowance of these claims are respectfully solicited.

With regard to independent claims 30 and 31, which are of similar scope, these claims recite an integrated circuit comprising "a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer . . . wherein the conductive layer comprises a plurality of conductive traces intersecting with and connecting to one another to form a net." As with claim 3, the Examiner acknowledges that Lim fails to disclose that the conductive layer comprises a plurality of conductive traces interconnected with one another to form a net (final Office Action; page 8, paragraph 3; page 9, last paragraph). However, the Examiner contends that such arrangement would be obvious. Applicant respectfully disagrees with this contention and submits that these claims are patentable over the prior art of record for at least the reasons set forth above in connection with claim 3. Accordingly, favorable reconsideration and allowance of claims 30 and 31 are respectfully requested.

In view of the foregoing, Applicant believes that claims 1-17 and 26-31 are in condition for allowance, and respectfully requests withdrawal of the §102(e) and §103(a) rejections.

As indicated above, a Notice of Appeal is being submitted.

Respectfully submitted,

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Enclosure(s): Notice of Appeal